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The present invention relates generally to the field of computer architecture, and more particularly to an apparatus and method for mapping a virtual address to a physical address. Hardware components of a computer system include a host which contains a processor, caches and a memory system. The host communicates with the memory system via a memory controller, which communicates with a memory bus. The memory bus transfers data to and from the memory system. With a memory based system, each memory access is typically referred to as a xe2x80x9creadxe2x80x9d or a xe2x80x9cwritexe2x80x9d access. A read access occurs when information is transferred to the processor from the memory system. The information is transferred by placing a bus request on the memory bus. In response to the bus request, the memory controller returns the requested information on the memory

bus. To transfer information from the memory system to the memory controller, the memory controller issues a bus request. In response to the bus request, the memory system transfers the requested information to the memory controller on the memory bus. A write access occurs when information is transferred from the processor to the memory system. The processor transfers information to the memory system in response to a bus request. In response to the bus request, the memory controller stores the information in the memory system and the memory controller returns an acknowledgement signal (ACK) to the processor. The CPU, the memory controller and the memory system are interconnected by a bi-directional bus. The bi-directional bus includes a system bus and a memory bus. The system bus is

coupled between the CPU and the memory controller and it serves as a communication channel for information to be transferred between the CPU and the memory controller. In contrast, the memory bus serves as a communication channel between the memory controller and the memory system. Processors are usually coupled to the system bus in a shared manner. That is, multiple processors may share access to the system bus. Memory systems usually couple memory components together in a shared manner. That is, each memory component usually serves as a memory for a subset of the system. For example, a memory component may be used to store the program code and operands of a program. The main memory often includes one or more caches, which are small high speed memory devices coupled to the system bus. For example, a cache is often added to a system to temporarily buffer frequently accessed instructions and data. The cache is usually implemented by semiconductor memory devices 04aeff104c

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